

September 26, 2001

To: Commissioner of Patents and Trademarks

Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572

20 McIntosh Drive

Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/905,408 07/16/01

Sheng Hsiung Chen, Mingh-Sing Tsai

SELECTIVE FORMATION OF METAL GATE FOR DUAL GATE OXIDE APPLICATION

Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,087,231 to Xiang et al., "Fabrication of Dual Gates of Field Transistors with Prevention of Reaction Between the Gate Electrode and the Gate Dielectric with a High Dielectric Constant," discloses a process for a dual gate.

TSMC-01-133

The following three U.S. Patents reveal processes for dual gates and dummy gates:

- 1) U.S. Patent 6,159,782 to Xiang et al., "Fabrication of Field Effect Transistors Havaing Dual Gates with Gate Dielectrics of High Dielectric Constant."
- 2) U.S. Patent 5,960,270 to Misra et al., "Method for Forming an MOS Transistor Having a Metallic Gate Electrode that is Formed After the Formation of Self-Aligned Source and Drain Regions."
- 3) U.S. Patent 6,043,157 to Gardner et al.,
 "Semiconductor Device Having Dual Gate Electrode
 Material and Process of Fabrication Thereof."

Sincerely

Stephen B. Ackerman,

Reg. No. 37761

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP \$609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.